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## REMARKS

At the outset, Applicants thank the Examiner for the thorough review and consideration of the subject application. The Non-Final Office Action of March 12, 2004 has been received and its contents carefully reviewed.

In the Non-Final Office Action of March 12, 2004, the Examiner objected to the specification due to various informalities; objected to the title as non-descriptive; rejected claims 15, 17-19, 22-29, 31, and 33-38 under 35 U.S.C. § 103(a) as being unpatentable over the related art shown in Figures 1A-1B in view of Hebiguchi (U.S. Patent No. 6,091,473) and Yao et al. (U.S. Patent No. 5,682,211); rejected claim 30 under 35 U.S.C. § 103(a) as being unpatentable over the related art shown in Figures 1A-1B in view of Hebiguchi and Yao et al. and further in view of Kouno et al. (U.S. Patent No. 5,818,560); and rejected claims 15, 17-19, 22-31, and 33-38 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,697,140. These rejections are traversed and reconsideration of the claims is respectfully requested in view of the following remarks.

Withdrawal of the objection to the specification is respectfully requested in view of the amendments made above, adopting the Examiner's suggestion.

While Applicants believe the title of the invention to be sufficiently descriptive, Applicants hereby amend the title of the invention solely for purposes of expediting prosecution. Accordingly, Applicants respectfully request the present objection to the title of the invention be withdrawn.

The rejection of claims 15, 17-19, 22-29, 31, and 33-38 under 35 U.S.C. § 103(a) as being unpatentable over the related art shown in Figures 1A-1B in view of Hebiguchi and Yao et al. is respectfully traversed and reconsideration is requested.

The present application is a continuation of prior application Serial No. 09/781,196, filed February 13, 2001 (which is now U.S. Patent No. 6,697,140). Application Serial No. 09/781,196 is a divisional of prior application Serial No. 09/235,205, filed January 21, 1999 (which is now U.S. Patent No. 6,445,435). Accordingly, the effective filing date of the present application is January 21, 1999. Further, the present application claims foreign priority under 35 U.S.C. § 119(a)-(d) to Korean Patent Application No. 98-2121, filed on January 23, 1998. Accordingly, Applicants hereby submit a certified English translation of Korean Patent Application No. 98-2121 to perfect the claim to foreign priority to Korean Patent Application

No. 98-2121 and respectfully submit Hebiguchi is not available as prior art. Even if the reference date of Hebiguchi antedated the present claim to foreign priority, Applicants respectfully submit the cited combination of the related art shown in Figures 1A-1B in view of Hebiguchi and Yao et al. still fails to teach each and every element as set forth in the claims. For at least these reasons, Applicants respectfully request withdrawal of the present rejection under 35 U.S.C. § 103(a).

The rejection of claim 30 under 35 U.S.C. § 103(a) as being unpatentable over the related art shown in Figures 1A-1B in view of Hebiguchi and Yao et al. and further in view of Kouno et al. is respectfully traversed and reconsideration is requested.

Claim 30 depends from independent claim 15 and, therefore, includes all of the features set forth in claim 15. As described above Hebiguchi does not constitute prior art with respect to the present application. Moreover, the related art shown in Figures 1A-1B in view of Hebiguchi and Yao et al. fails to teach at least the features set forth in claim 15. Even if Kouno et al. discloses the various features asserted by the Examiner, and even if Kouno et al. could be combined with the related art shown in Figures 1A-1B in view of Hebiguchi and Yao et al. as suggested by the Examiner, Applicants respectfully submit that Kouno et al. fails to cure the deficiencies of the related art shown in Figures 1A-1B in view of Hebiguchi and Yao et al. with respect to claim 15. Accordingly, Applicants submit that claim 30 is allowable over the Examiner's cited combination of the related art shown in Figures 1A-1B in view of Hebiguchi and Yao et al. and further in view of Kouno et al. by virtue of its dependence from claim 15 and request withdrawal of the present rejection under 35 U.S.C. § 103(a).

The rejection of claims 15, 17-19, 22-31, and 33-38 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,697,140 is respectfully traversed and reconsideration is requested.

Applicants disagree with the rationale underlying the obviousness-type double patenting rejection of claims 15, 17-19, 22-31, and 33-38 in view of claims 1-6 of U.S. Patent No. 6,697,140. However, for the sole purpose of expediting prosecution, Applicants hereby submit a terminal disclaimer of U.S. Patent No. 6,697,140 and request withdrawal of the present obviousness-type double patenting rejection.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If the Examiner deems that a telephone conversation would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7500.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

Dated: June 14, 2004

Respectfully submitted,

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(Translation)

# THE KOREAN INDUSTRIAL PROPERTY OFFICE

This is to certify that the following application annexed hereto is a true copy from the records of the Korean Industrial Property Office.

Application Number : Patent Application 2121/1998

Date of Application : January 23, 1998

Applicant : LG Electronics Inc.

Commissioner

(Translation)

[Document Name] Written Application for Patent
[Attention] Commissioner of the Korean Industrial Property Office
[Filing Date ] January 23, 1998
[Title of Device] IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE

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# CERTIFICATE OF VERIFICATION

I, Su Hyun LEE of 648-23 Yeoksam-dong, Kangnam-ku, Seoul, Korea state that the attached document is a true and complete translation to the best of my knowledge of the Korean-English language and that the writings contained in the following pages are correct English translations of the specifications and claims of the Korean Patent Application No. P1998-2121.

Dated this 9th day of June, 2004

Signature of translator: _____

Su Hyun LEE

[ABSTRACT]

An IPS mode LCD device is disclosed, which includes first and second substrates; a plurality of gate and data lines crossing each other on the first substrate; a plurality of thin film transistor at respective crossing points of the plurality of gate and data lines; a plurality of data electrodes on the same plane as the data lines, having one portion overlapped with the adjacent gate line; a passivation layer on the thin film transistor and the data electrode; a plurality of common electrodes which are substantially parallel to the data electrode on the passivation layer and covering the n-th numbered gate line and the (n+1)-th numbered gate line, or the n-th numbered gate line and the (n-1)-th numbered gate line; a common line which is formed on the same plane as the common electrode and covering the n-th numbered gate line and the (n+1)-th numbered gate line or the n-th numbered gate line and the (n-1)-th numbered gate line; a first alignment layer on the common electrode, a black matrix layer on the second substrate to prevent light leakage through the regions of the thin film transistor, the gate line, the data line and the common line; a color filter layer and a second alignment layer on the black matrix layer, and a liquid crystal layer between the first and second substrates, wherein a storage capacitor is formed by an overlap region of the gate line, the data electrode, the common electrode or the common line.

[TYPICAL DRAWINGS]

FIG. 2

**[SPECIFICATION]**

**[TITLE OF THE INVENTION]**

IN-PLANE SWITCHING MODE LIQUID CRYSTAL DISPLAY DEVICE

**[BRIEF DESCRIPTION OF THE DRAWINGS]**

FIG. 1A is a plane view illustrating a unit pixel of a related art IPS mode LCD device.

FIG. 1B is a cross-sectional view taken along line A-A' of FIG. 1A.

FIG. 2A is a plane view illustrating a unit pixel of an IPS mode LCD device according to one preferred embodiment of the present invention.

FIG. 2B is a cross-sectional view taken along line B-B' of FIG. 2A.

FIG. 3A is a plane view illustrating a unit pixel of an IPS mode LCD device according to another embodiment of the present invention.

FIG. 3B is a cross-sectional view taken along line C-C' of FIG. 3A.

***Description of reference numerals for main parts in the drawings***

| | |
|---|---|
| 101: gate line | 102: data line |
| 103: common line | 106: source electrode |
| 107: drain electrode | 108: data electrode |
| 109: common electrode | 110: first substrate |
| 111: second substrate | 112: gate insulating layer |
| 115: semiconductor layer | 120: passivation layer |
| 123: alignment layer | 128: black matrix layer |
| 129: color filter layer | 130: liquid crystal layer |

**[DETAILED DESCRIPTION OF THE INVENTION]**

**[OBJECT OF THE INVENTION]**

**[FIELD OF THE INVENTION AND DISCUSSION OF THE RELATED ART]**

The present invention relates to a liquid crystal display (LCD) device, and more particularly, to an In-Plane switching (IPS) mode LCD device having a high aperture ratio.

Recently, according as the thin film transistor liquid crystal display devices (TFT-LCDs) have been used as display devices in such applications as portable televisions and notebook computers, it is strongly required to obtain large-sized TFT-LCDs. However, the TFT-LCDs have the problem in that the contrast ratio is changed according to change of viewing angle. In order to solve this problem, twisted nematic LCDs having, for example, optical compensation plates and multi-domains, have been introduced. In these LCDs, however, the color of the image is shifted because the contrast ratio depends on the viewing angle direction.

For a wide viewing angle, the In-Plane switching mode LCD is disclosed, for example, in JAPAN DISPLAY 92 P547, Japanese Patent Unexamined Publication No. 7-36058, Japanese Patent Unexamined Publication No. 7-225538, and ASIA DISPLAY 95 P107.

FIG. 1A is a plane view illustrating a unit pixel of a related art IPS mode LCD device. FIG. 1B is a cross-sectional view taken along line A-A' of FIG. 1A. The related art IPS mode LCD device includes gate and data lines 1 and 2 formed on a first substrate 10 to define a pixel region, a common line 3 arranged in the pixel region for being in parallel to the gate line 1, a thin film transistor formed at a crossing point of the

gate and data lines 1 and 2, and data and common electrodes 8 and 9 formed in the pixel region for being parallel to the data line 2. Also, the thin film transistor includes a gate electrode 5 formed on the first substrate 10 for being in contact with the gate line 1, a gate insulating layer 12 deposited on the gate electrode 5, an active layer 15 formed on the gate insulating layer 12, and source and drain electrodes 6 and 7 formed on the active layer 15 for being in contact with the data line 2 and the data electrode 8. The common electrode 9 of the pixel region is formed on the first substrate 10 for being in contact with the common line 3, and the data electrode 8 is formed on the gate insulating layer 12 for being in contact with the drain electrode 7 of the thin film transistor. Then, a passivation layer 20 is formed on the thin film transistor and entire portions within the pixel region, and a first alignment layer 23a is deposited on an entire surface of the first substrate 10.

On the second substrate 11, a black matrix layer 28 is formed to prevent light leakage through the regions of the thin film transistor, the gate line 1, the data line 2 and the common line 3. Then, a color filter layer 29 and a second alignment layer 23b are formed thereon. Also, a liquid crystal layer 30 is formed between the first and second substrates 10 and 11.

In the aforementioned IPS mode LCD device, an electric field being in parallel to the first and second substrates 10 and 11 is generated between the data and common electrodes 8 and 9 when a voltage is supplied from an external driving circuit. Accordingly, liquid crystal molecules aligned in the liquid crystal layer 30 are rotated according the electric field, thereby controlling the amount of light passing through the liquid crystal layer 30.

Generally, the LCD device uses a storage capacitor to improve the maintenance

characteristics of the liquid crystal applying voltage, to obtain the stable gray level, and to prevent flicker and residual images. Methods of forming the storage capacitor are classified into an SOG (Storage On Gate) mode and an SOC (Storage On Common) mode. In the SOG mode, some part of the (n-1)-th numbered gate line is applied as a storage capacitor in the n-th numbered pixel region. In the SOC mode, a separate electrode for storage capacitor is electrically coupled to the common electrode.

By using the storage capacitor, the aperture ratio is decreased, and the metal lines are in the short state, thereby decreasing yield.

**[TECHNICAL TASKS TO BE ACHIEVED BY THE INVENTION]**

An object of the present invention is to provide an IPS mode LCD device having high aperture ratio and high yield in a method of using an SOG mode, or both SOG and SOC modes by forming a gate electrode, a data electrode and a common electrode on different planes.

To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, an IPS mode LCD device includes first and second substrates; a plurality of gate and data lines crossing each other on the first substrate; a plurality of thin film transistor at respective crossing points of the plurality of gate and data lines; a plurality of data electrodes on the same plane as the data lines, having one portion overlapped with the adjacent gate line; a passivation layer on an entire surface of the first substrate including the thin film transistor and the data electrode; a plurality of common electrodes which are substantially parallel to the data electrode on the passivation layer and covering the n-th numbered gate line and the (n+1)-th numbered gate line, or the n-th numbered gate line

and the (n-1)-th numbered gate line; a common line which is formed on the same plane as the common electrode and covering the n-th numbered gate line and the (n+1)-th numbered gate line or the n-th numbered gate line and the (n-1)-th numbered gate line; a first alignment layer on the common electrode, a black matrix layer on the second substrate to prevent light leakage through the regions of the thin film transistor, the gate line, the data line and the common line; a color filter layer and a second alignment layer on the black matrix layer, and a liquid crystal layer between the first and second substrates, wherein a storage capacitor is formed by an overlap region of the gate line, the data electrode, the common electrode or the common line.

In another aspect, a data electrode is formed on the same plane as a data line, and has one portion overlapped with the adjacent n-th numbered gate line. Also, a common electrode has one portion overlapped with the adjacent data electrode, and the other portion not to be overlapped with the opposing data electrode and the (n+1)-th numbered gate line, wherein a storage capacitor is formed by an overlap region of the gate line, the data electrode, the common electrode or the common line.

**[PREFERRED EMBODIMENTS OF THE INVENTION]**

Hereinafter, an IPS mode LCD device according to the present invention will be described with reference to the accompanying drawings.

FIG. 2A is a plane view illustrating a unit pixel of an IPS mode LCD device according to one preferred embodiment of the present invention. FIG. 2B is a cross-sectional view taken along line B-B' of FIG. 2A. As shown in the drawings, a plurality of gate lines 101 and 101' and a data line 102 are arranged perpendicularly and/or horizontally in a matrix type on a first substrate 110. The drawings only show a

unit pixel region. Actually, the LCD device has a plurality of pixel regions of n×m including a large number of gate lines (n) and data lines (m).

A gate insulating layer 112 is deposited on the gate lines 101 and 101'. The gate lines 101 and 101' act as a gate electrode of a thin film transistor. At this time, a metal layer of Al, Mo, Ta, Cr or Al alloy is deposited at a thickness of approx. 3000Å by sputtering, and then etched, thereby forming the gate lines 101 and 101'. Meanwhile, the gate insulating layer 112 is formed in a method of depositing an inorganic layer of $SiN_x$ or $SiO_x$ by CVD (Chemical Vapor Deposition).

After that, a semiconductor layer 115 is formed on the gate insulating layer 112. The semiconductor layer 115 acts as a channel layer, which is formed by depositing an amorphous silicon layer (a-Si) by CVD, and etching the deposited a-Si layer. Thereafter, an ohmic contact layer 116 of $n^+$ a-Si is formed on the semiconductor layer 115. Also, the data line 102, a source electrode 106, a drain electrode 107 and a data electrode 108 are formed on the ohmic contact layer 116 and the gate insulating layer 112. At this time, a metal layer of Al, Cr, Ti or Al alloy is deposited at a thickness of approx. 1000Å by sputtering, and then etched, thereby forming the data line 102, the source electrode 106, the drain electrode 107 and the data electrode 108. In another method, after pattering the gate line of Al, the gate electrode of Cr is patterned. After that, on the substrate having the patterned gate line thereon, the gate insulating layer, the semiconductor layer and impurity semiconductor layer are formed in sequence. Then, the ohmic contact layer is formed in a method of patterning the impurity semiconductor layer. Thereafter, after opening a pad, the source and drain electrodes of Cr are deposited and patterned, thereby forming the data electrode.

Also, an inorganic material such as $SiN_x$ or $SiO_x$ or an organic material such as

BCB (BenzoCycloButene) is deposited on a thin film transistor, the data line 102, the data electrode 108 and the gate insulating layer 112, thereby forming a passivation layer 120. Subsequently, after opening the pad, a metal layer of Al, Mo, Ta, ITO or Al alloy is deposited on the passivation layer 120, and then patterned, thereby forming a common electrode 109 and a common line 103. Thereon, a first alignment layer 123a is formed. At this time, the data line 102 is formed on the same plane as the data electrode 108, and some of the data line 102 is formed on the gate line 101. Also, the common electrode 109 that is substantially parallel to the data electrode 108 is formed on the gate lines 101 and 101', and this is applied to the adjacent pixel region.

The reference number 125 represents an electrode for storage capacitor, which is formed by overlapping the gate electrode, the data electrode and the common electrode at the different layers.

In the present invention, the storage capacitor is formed by the plurality of common electrodes 109 which are substantially parallel to the data electrode 108 on the passivation layer 120 and covers the n-th numbered gate line and the (n+1)-th numbered gate line, or the n-th numbered gate line and the (n-1)-th numbered gate line, and the common line 103 which is formed on the same plane as the common electrode 109 and covers the n-th numbered gate line and the (n+1)-th numbered gate line or the n-th numbered gate line and the (n-1)-th numbered gate line.

After that, the first alignment layer 123a is formed of a photo-reactive material such as polyimide, PVCN (polyvinylcinnamate)-based material or polysiloxane-based material, on the passivation layer 120 and the common electrode 109. In case the first alignment layer 123a is formed of polyimide, an alignment direction thereof is determined by mechanical rubbing. In case the first alignment layer 123a is formed of

the photo-reactive material such as PVCN (polyvinylcinnamate) or polysiloxane-based materials, an alignment direction thereof is determined by irradiation of ultraviolet light. The alignment direction of the first alignment layer may be changed according to the peculiar characteristics of light such as the polarizing direction of light. In case of using the mechanical rubbing, it is possible to solve the problem of dusts or static electricity on the alignment layer.

On the second substrate 111, a black matrix layer 128 is formed to prevent leakage of light through the regions of the thin film transistor, the gate line 101, the data line 102 and the common line 103. Also, a color filter layer 129 and a second alignment layer 123b are formed on the black matrix layer 128. Thereafter, a liquid crystal layer 130 is formed between the first and second substrates 110 and 111, thereby completing the IPS mode LCD device according to the present invention.

At this time, the black matrix layer 128 is formed in a method of etching Cr or CrOx layer deposited by sputtering, and the color filter layer 129 is formed in a method of repetitively forming R/G/B layers in the respective pixel regions. Then, the second alignment layer 123b of polyimide or photo-reactive material is formed on the color filter layer 129 by rubbing or light irradiation, thereby determining the alignment direction.

FIG. 3A is a plane view illustrating a unit pixel of an IPS mode LCD device according to another embodiment of the present invention. FIG. 3B is a cross-sectional view taken along line C-C' of FIG. 3A.

Referring to FIG. 3A and FIG. 3B, the IPS mode LCD device according to the second embodiment of the present invention is different from the IPS mode LCD device according to the first embodiment of the present invention in that the common electrode

109 covers some part of the pixel electrode 108, and does not cover the gate line 101.

**[ADVANTAGES OF THE INVENTION]**

As mentioned above, the IPS mode LCD device according to the present invention has the following advantages.

In the IPS mode LCD device according to the present invention, the gate electrode, the data electrode and the common electrode are formed on the different planes, whereby it is possible to prevent the short state between the electrodes, the short state generated by forming the gate electrode and the common electrode on the same plane, thereby improving yield. By using the SOG mode, or both SOG and SOC modes, it is possible to provide the IPS mode LCD device having the high aperture ratio, without covering some of open part.

**What is claimed is:**

1. An IPS mode LCD device comprising:

first and second substrates;

a plurality of gate and data lines crossing each other on the first substrate, to define pixel regions;

a plurality of thin film transistor at respective crossing points of the plurality of gate and data lines;

a plurality of data electrodes on the same plane as the data lines, having one portion overlapped with the adjacent gate line;

a passivation layer on an entire surface of the first substrate including the thin film transistor and the data electrode;

a plurality of common electrodes on the passivation layer, having some part overlapped with the adjacent two gate lines, and applied to the adjacent pixel region; and

a liquid crystal layer between the first and second substrates.

2. The IPS mode LCD device of claim 1, wherein the gate line, the data electrode and the common electrode are overlapped to form a storage capacitor.

3. The IPS mode LCD device of claim 1, wherein the thin film transistor includes:

the gate line;

a gate insulating layer deposited on the gate line;

a semiconductor layer formed on the gate line; and

source and drain electrodes on the semiconductor layer.

4. The IPS mode LCD device of claim 1, further comprising:

a common line formed in the pixel region of the first substrate, to be in contact with the common electrode; and

a black matrix layer formed on the second substrate along the gate line of the first substrate.

5. The IPS mode LCD device of claim 4, wherein the common line is formed on the passivation layer.

6. The IPS mode LCD device of claim 1, further comprising:

a first alignment layer deposited on the first substrate;

a color filter layer formed on the second substrate; and

a second alignment layer deposited on the second substrate and the color filter layer.

7. The IPS mode LCD device of claim 6, wherein the first alignment layer or the second alignment layer is formed of polyimide.

8. The IPS mode LCD device of claim 6, wherein the first alignment layer or the second alignment layer is formed of photo-reactive material.

9. The IPS mode LCD device of claim 8, wherein the photo-reactive material is formed of any one of PVCN (polyvinylcinnamate)-based material or polysiloxane-based material.

10. An IPS mode LCD device comprising:

first and second substrates;

a plurality of gate and data lines crossing each other on the first substrate, to define pixel regions;

a plurality of thin film transistor at respective crossing points of the plurality of gate and data lines;

a plurality of data electrodes on the same plane as the data lines, having one portion overlapped with the adjacent gate line;

a passivation layer on an entire surface of the first substrate including the thin film transistor and the data electrode;

a plurality of common electrodes on the passivation layer, having one portion overlapped with the adjacent data electrode, and the other portion being in contact with an overlap portion between the gate line and the data electrode; and

a liquid crystal layer between the first and second substrates.

11. The IPS mode LCD device of claim 10, wherein a storage capacitor is formed by the overlap portion of the gate line and the data electrode, and the common electrode being adjacent to the overlap portion.

FIG. 1

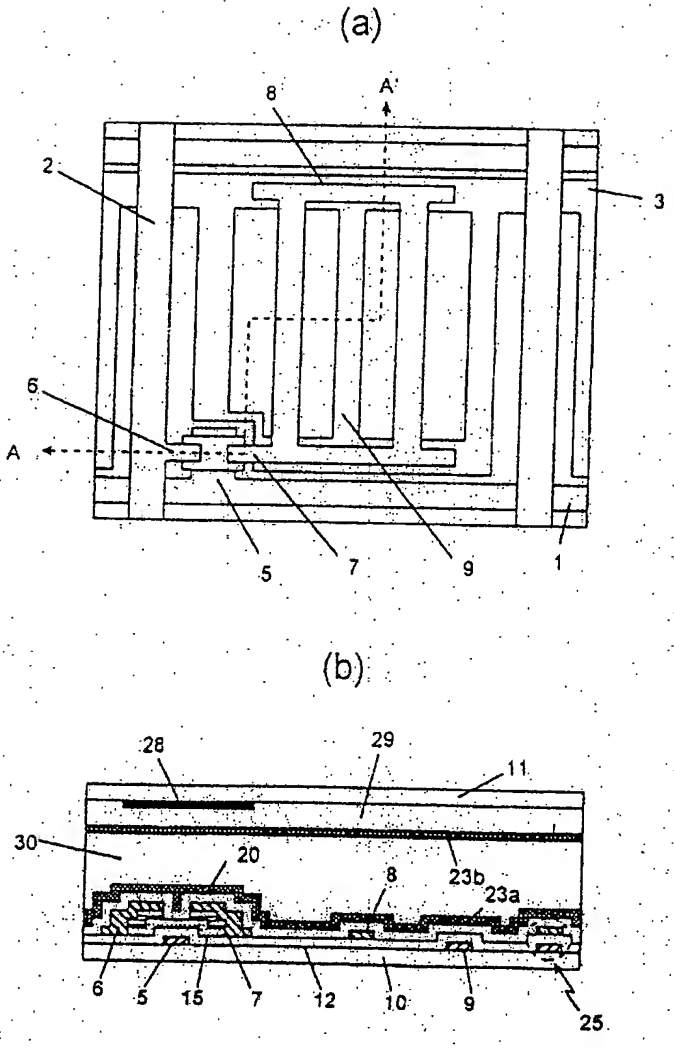
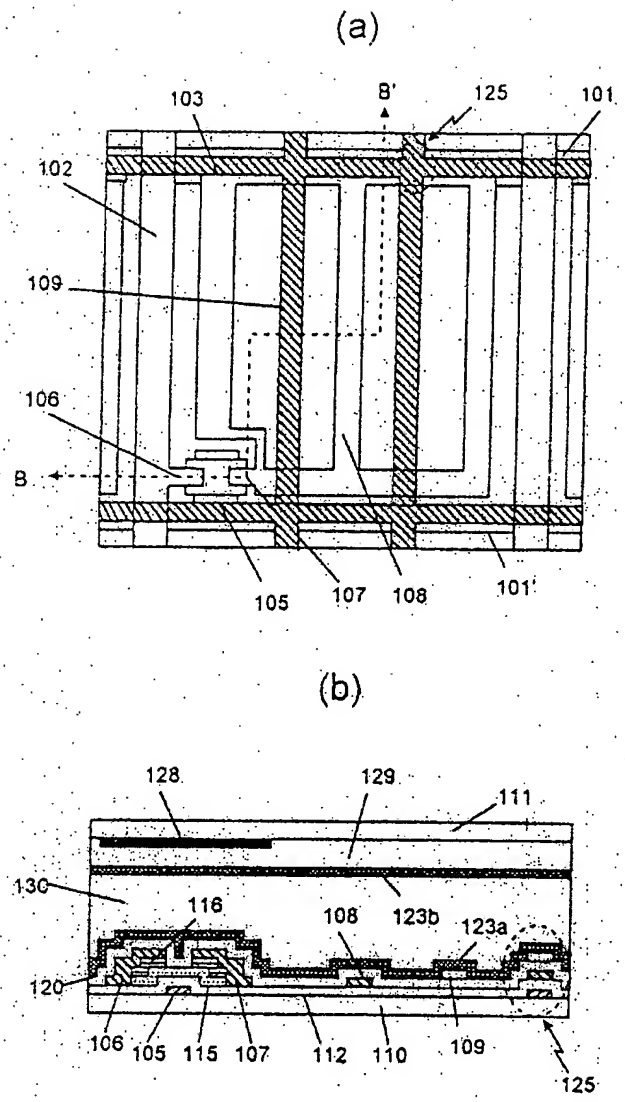


FIG. 2


(a)
103
B'
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101
102
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107
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101'
(b)
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123b
123a
120
106
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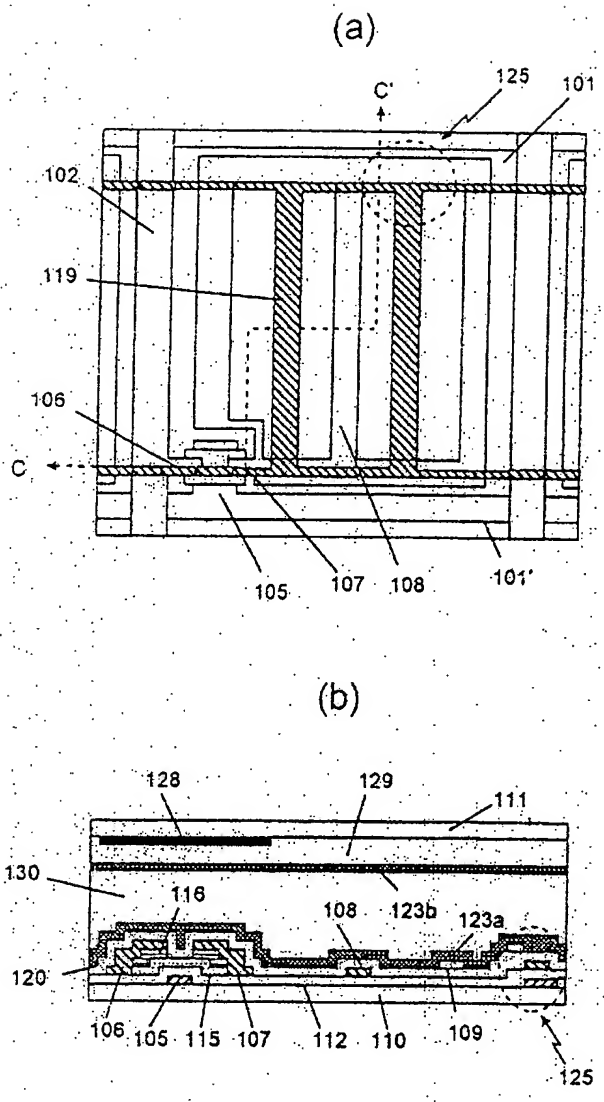
107
112
110
109
125

FIG. 3


(a)
C'
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